Course Code : 210
Section: B1

"Digital Logic Design Lab

Project : 01

Problem Statement : Design & Implement a 5-bit synchronous counter for the following pattern 0.2.3.5.7.11.13.17.23.29.30.31.0

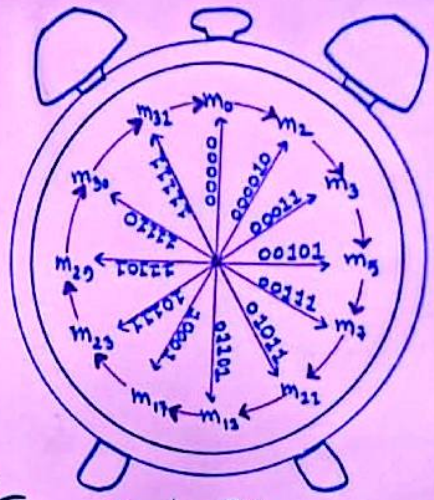
Transition Excitation truth table of a J-K Flip Flop

Output Transition		F.F Transition	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

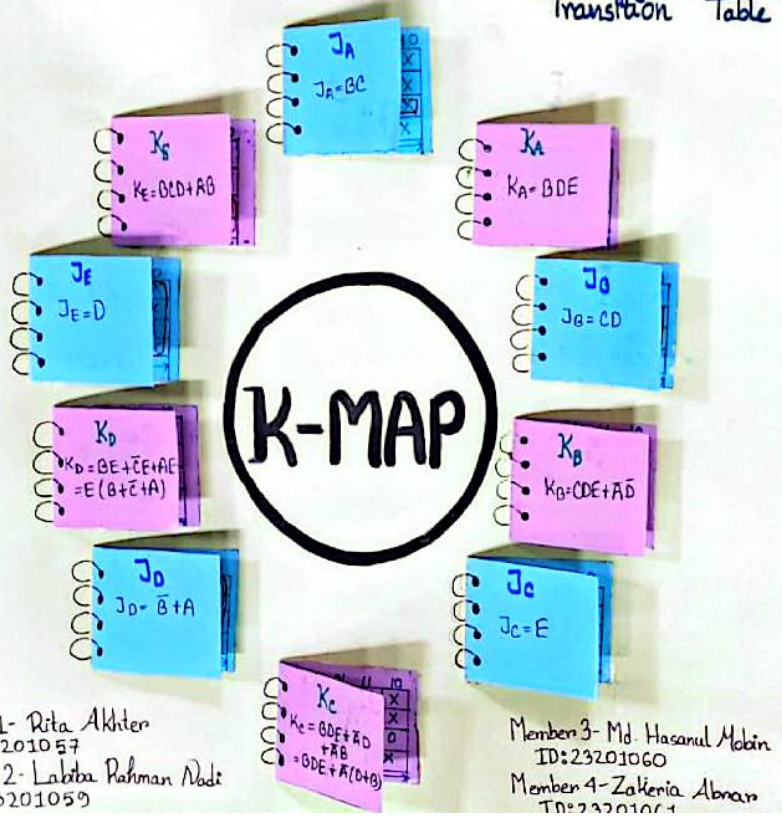
Present State					Next State					A		B		C		D		E	
Q_A	Q_B	Q_C	Q_D	Q_E	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D	J_E	K_E
0	0	0	0	0	0	0	0	1	0	0	X	0	X	0	X	1	X	0	X
0	0	0	1	0	0	0	0	1	1	0	X	0	X	0	X	X	0	1	X
0	0	0	1	1	0	0	1	0	1	0	X	0	X	1	X	X	1	X	0
0	0	1	0	1	0	0	1	1	1	0	X	0	X	X	0	1	X	X	0
0	0	1	1	1	0	1	0	1	1	0	X	1	X	X	1	X	0	X	0
0	1	0	1	1	0	1	1	0	1	0	X	X	0	1	X	X	1	X	0
0	1	1	0	1	1	0	0	0	1	1	X	X	1	X	1	0	X	X	0
1	0	0	0	1	1	0	1	1	1	X	0	0	X	1	X	1	X	X	0
1	0	1	1	1	1	1	1	0	1	X	0	1	X	X	0	X	1	X	0
1	1	1	0	1	1	1	1	1	0	X	0	X	0	X	0	1	X	X	1
1	1	1	1	0	1	1	1	1	1	X	0	X	0	X	0	X	0	1	X
1	1	1	1	1	0	0	0	0	0	X	1	X	1	X	1	X	1	X	1

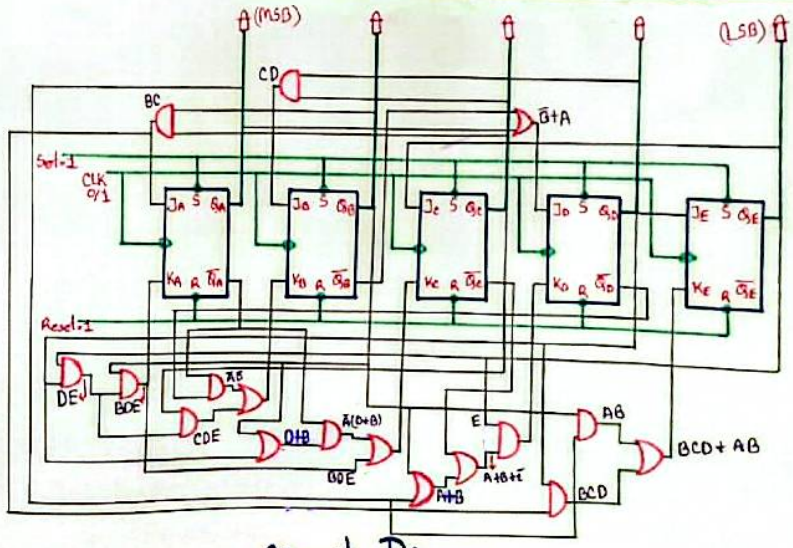
Transition Table

State Diagram :



"From 0 to 31..... but our way!!"





Circuit Diagram

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